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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/740,530	12/18/2000	Michael S. Floyd	AUS920000710US1 (9000/4)	8384

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EXAMINER	
MCCARTHY, CHRISTOPHER S	

ART UNIT	PAPER NUMBER
2113	10

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No. 09/740,530	Applicant(s) FLOYD ET AL.
	Examiner Christopher S. McCarthy	Art Unit 2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *40 and 43* is/are allowed.

6)☒ Claim(s) *1-4,7,8,11-14,17,18,21,22,24,26-29,31-33,36,37,39,41 and 42* is/are rejected.

7)☒ Claim(s) *5,6,9,10,15,16,19,20,23,25,30,34,35 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *11* .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☒ Other: *Response to arguments*.

DETAILED ACTION

1. Claims 1-4, 7-8, 11-14, 17-18, 21-22, 24, 26-29, 31-33, 36-37, 39, 41, and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Miyamori et al U.S. Patent 5,978,937, as cited in prior office action, which was mailed on 2/3/2004.

2. Claims 40, and 43 are allowed, as cited in prior office action, which was mailed on 2/3/2004.

3. Claims 5, 6, 9, 10, 15-16, 19-20, 23, 25, 30, 34-35, 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, as cited in prior office action, which was mailed on 2/3/2004.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 7-8, 11-14, 17-18, 21-22, 24, 26-29, 31-33, 36-37, 39, 41, and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Miyamori et al U.S. Patent 5,978,937.

As per claim 1, Miyamori teaches a method for transitioning a debugging unit between a plurality of operating states, comprising defining a first set of operating instructions to be processed by a processor core; defining a first triggering instruction to provide a first signal to

the debugging unit whereby the debugging unit is operable to transition from a first operating state to a second operating state; and embedding said first triggering instruction within said first set of operating instructions (column 5, line 54 – column 6, line 20), wherein, the triggering instruction is inclusive in the executed program stream as used in Miyamori.

As per claim 2, Miyamori teaches the method of claim 1, further comprising of coding said first set of operating instructions within a computer readable medium, said coded first set of operating instructions including a coded first triggering instruction; operating said computer readable medium to provide an instruction stream to a processor core, said instruction stream representative of said coded first set of operating instructions, said instruction stream including a second signal representative of said coded first triggering instruction; and operating said processor core to provide said first signal to the debugging unit in response to said second signal to thereby transition the debugging unit from the first operating state to the second operating state (column 5, line 54 – column 6, line 20), wherein it is inherent that a computer coded language is used in the programming of the Miyamori invention. Also, the signals of the present claim are interpreted as the same in the Miyamori, wherein a signal is inherent in the program instructions executed by the core and another signal is present in the instruction from the core to the debugging unit.

As per claim 3, Miyamori teaches the method of claim 1, further comprising of defining a second triggering instruction to provide a second signal to the debugging unit whereby the debugging unit is operable to transition from the second operating state to the first operating state; and embedding said second triggering instruction within said first set of operating

instructions (column 6, lines 17-20, 52-54), wherein, the debugger is transitioned from the second state to the first state when the reset instruction (signal) is executed.

As per claim 4, Miyamori teaches the method of claim 3, further comprising of coding said first set of operating instructions within a computer readable medium, said coded first set of operating instructions including a coded first triggering instruction and a coded second triggering instruction; operating said computer readable medium to provide an instruction stream to a processor core, said instruction stream representative of said coded first set of operating instructions, said instruction stream including a third signal representative of said coded first triggering instruction and a fourth signal representative of said coded second triggering instruction; operating said processor core to provide said first signal to the debugging unit in response to said third signal to thereby transition the debugging unit from the first operating state to the second operating state; and subsequent to providing said first signal to the debugging unit, operating said processor core to provide said second signal to the debugging unit in response to said fourth signal to thereby transition the debugging unit from the second operating state to the first operating state (column 5, line 54 – column 6, line 20; column 6, lines 17-20, 52-54), wherein it is inherent that a computer coded language is used in the programming of the Miyamori invention. Also, the signals of the present claim are interpreted as the same in Miyamori, wherein a signal is inherent in the program instructions executed by the core and another signal is present from the core to the debugging unit.

As per claim 7, Miyamori teaches the method of claim 1, further comprising of defining a second set of operating instructions to generate a first data or a second data; and embedding said

second set of operating instructions within said first set of operating instructions (column 6, lines 17-20).

As per claim 8, Miyamori teaches the method of claim 7, further comprising of coding said first set of operating instructions within a computer readable medium, said first set of operating instructions including a coded first triggering instruction and a coded second set of operating instructions; operating said computer readable medium to provide an instruction stream to a processor core, said instruction stream representative of said coded first set of operating instructions, said instruction stream including a second signal representative of said coded first triggering instruction and a set of signals representative of said coded second set of operating instructions; operating said processor core to generate said first data or said second data in response to said set of signals; and subsequent to a generation of said first data by said processor core, operating said processor core to provide said first signal to the debugging unit in response to said second signal to thereby transition the debugging unit from the first operating state to the second operating state (column 5, line 54 – column 6, line 20; column 6, lines 17-20, 52-54), wherein it is inherent that a computer coded language is used in the programming of the Miyamori invention. Also, the signals of the present claim are interpreted as the same in Miyamori, wherein a signal is inherent in the program instructions executed by the core and another signal is present from the core to the debugging unit.

As per claim 11, Miyamori teaches a microprocessor, comprising a debugging unit operable to transition from a first operating state to a second operating state in response to a first signal; and a processor core operable to fetch an instruction stream including a second signal representative of a first triggering instruction to transition said debugging unit from said first

operating state to said second operating state, said processor core further operable to provide said first signal to said debugging unit in response to said second signal (column 5, line 54 – column 6, line 20).

As per claim 12, Miyamori teaches the microprocessor of claim 11, wherein said processor core includes a register operable to provide said first signal to said debugging unit in response to a third signal including an address of said register (column 5, line 54 – column 6, line 20; column 7, lines 13-23, 39-46).

As per claim 13, Miyamori teaches the microprocessor of claim 11, wherein said debugging unit is further operable to transition from said second operating state to said first operating state in response to a third signal; said instruction stream further includes a fourth signal representative of a second triggering instruction to transition said debugging unit from said second operating state to said first operating state; and said processor core is further operable to provide said third signal to said debugging unit in response to said fourth signal (column 5, line 54 – column 6, line 20; column 6, lines 17-20, 52-54),), wherein, the debugger is transitioned from the second state to the first state when the reset instruction (signal) is executed.

As per claim 14, Miyamori teaches the microprocessor of claim 13, wherein said processor core includes a first register operable to provide said first signal to said debugging unit in response to a fifth signal including an address of said first register; and a second register operable to provide said third signal to said debugging unit in response to a sixth signal including an address of said second register (column 7, lines 13-23, 39-46), wherein, Miyamori teaches multiple control registers in the processor for exception addresses pertaining to the debugger.

As per claim 17, Miyamori teaches the microprocessor of claim 11, wherein said instruction stream further includes a set of signals representative of a set of operating instructions to operate said processor core to generate a first data or a second data; said processor core is further operable to generate said first data or said second data in response to said set of signals; and subsequent to a generation of said trigger data, said processor core is further operable to provide said first signal to said debugging unit in response to said second signal (column 5, line 54 – column 6, line 20; column 6, lines 17-20). Also, the signals of the present claim are interpreted as the same in Miyamori, wherein a signal is inherent in the program instructions executed by the core and another signal is present from the core to the debugging unit.

As per claim 18, Miyamori teaches the microprocessor of claim 17, wherein said processor core includes a register operable to provide said second signal to said debugging unit in response to a third signal including an address of said register and a fourth signal including said first data (column 5, line 54 – column 6, line 20; column 7, lines 13-23, 39-46).

As per claim 21, Miyamori teaches a computer readable medium storing a program for transitioning a debugging unit between a plurality of operating states, comprising of a first computer readable code to operate a processor core; and a second computer readable code to transition the debugging unit from a first operating state to a second operating state, said second computer readable code embedded within said first computer readable code (column 5, line 54 – column 6, line 20), wherein it is inherent that a computer coded language is used in the programming of the Miyamori invention.

As per claim 22, Miyamori teaches the computer readable medium of claim 21, further comprising of a third computer readable code to transition the debugging unit from said second

operating state to said first operating state, said third computer readable code embedded within said first computer readable code (column 6, lines 17-20, 52-54).

As per claim 24, Miyamori teaches the computer readable medium of claim 21, further comprising a third computer readable code to operate said processor core to generate a first data or a second data, said third computer readable code embedded within said first computer readable code, wherein said second computer readable code is to transition the debugging unit from said first operating state to said second operating state in response to a generation of said first data (column 5, line 54 – column 6, line 20; column 6, lines 17-20).

As per claim 26, Miyamori teaches a system for transitioning a debugging unit between a plurality of operating states, comprising of a computer readable medium including a first computer readable code to transition the debugging unit from a first operating state to a second operating state, said computer readable medium operable to provide a first signal representative of said first computer readable code; and a processor core operable to provide a second signal to the debugging unit in response to said first signal whereby the debugging unit is operable to transition from the first operating state to the second operating state (column 5, line 54 – column 6, line 20), wherein it is inherent that a computer coded language is used in the programming of the Miyamori invention.

As per claim 27, Miyamori teaches the system of claim 26, wherein said processor core includes a register operable to provide said second signal in response to a third signal including an address of said register (column 5, line 54 – column 6, line 20; column 7, lines 13-23, 39-46).

As per claim 28, Miyamori teaches the system of claim 27, wherein said computer readable medium further includes a second computer readable code to transition the debugging

unit from the second operating state to the first operating state, said computer readable medium operable to provide a third signal representative of said second computer readable code; and said processor core is further operable to provide a fourth signal to the debugging unit in response to said third signal whereby the debugging unit is operable to transition from the second operating state to the first operating state (column 5, line 54 – column 6, line 20; column 6, lines 17-20, 52-54).

As per claim 29, Miyamori teaches the system of claim 28, wherein said processor core includes a first register operable to provide said second signal to the debugging unit in response to a fifth signal including an address of said first register; and a second register operable to provide said fourth signal to the debugging unit in response to a sixth signal including an address of said second register (column 7, lines 13-23, 39-46), wherein, Miyamori teaches multiple control registers in the processor for exception addresses pertaining to the debugger.

As per claim 31, Miyamori teaches the system of claim 30, wherein said processor core includes a first register operable to provide said second signal to the debugging unit in response to a fifth signal including an address of said first register; and a second register operable to provide said fourth signal to the debugging unit in response to a sixth signal including an address of said second register (column 5, line 54 – column 6, line 20), wherein, Miyamori teaches multiple control registers in the processor for exception addresses pertaining to the debugger.

As per claim 32, Miyamori teaches the system of claim 27, wherein said computer readable medium further includes a second computer readable code to operate said processor core to generate a first trigger data or a second trigger data, said computer readable medium operable to provide a set of signals representative of said second computer readable code; said

processor core is further operable to selectively generate said trigger data in response to said set of signals; and subsequent to a generation of said first data, said processor core is operable to provide said first signal to the debugging unit in response to said second signal (column 5, line 54 – column 6, line 20).

As per claim 33, Miyamori teaches the system of claim 32, wherein said processor core includes a register operable to provide said second signal to the debugging unit in response to a third signal including an address of said register and a fourth signal including said trigger data (column 5, line 54 – column 6, line 20; column 7, lines 39-46).

As per claim 36, Miyamori teaches a method for transitioning a debugging unit between a plurality of operating states, comprising of receiving a first signal representative of a first triggering instruction to transition the debugging unit from a first operating state to a second operating state; and processing said first signal to thereby transition the debugging unit from said first operating state to said second operating state (column 5, line 54 – column 6, line 20).

As per claim 37, Miyamori teaches the method of claim 36, receiving a second signal representative of a second triggering instruction to transition the debugging unit from said second operating state to said first operating state; and processing said second signal to thereby transition the debugging unit from said second operating state to said first operating state (column 6, lines 17-20, 52-54).

As per claim 39, Miyamori teaches a method for transitioning a debugging unit between a plurality of operating states, comprising of receiving a set of operating signals representative of a set of operating instructions to generate a first data or a second data; receiving a trigger

instruction signal representative of a triggering instruction to transition the debugging unit from a first operating state to a second operating state in response to a generation of said first data; and 10 processing said set of operating signals and said trigger instruction signal to thereby transition the debugging unit from said first operating state to said second operating state in response to a generation of said first data (column 5, line 54 – column 6, line 20).

As per claim 41, Miyamori teaches a method, comprising of providing a computer readable medium operable to provide a first signal representative of a first triggering instruction to transition a debugging unit from a first operating state to a second operating state; providing a processor core operable to provide a second signal in response to said first signal; and providing a debugging unit operable to transition from said first operating state to said second operating state in response to said second signal (column 5, line 54 – column 6, line 20).

As per claim 42, Miyamori teaches a method, comprising: providing a computer readable medium operable to provide a set of operating signals representative of a set of operating instructions to generate a first data or a second data, and a trigger instruction signal representative of a triggering instruction to transition a debugging unit from a first operating state to a second operating; providing a processor core operable to generate said first data or said second data in response to said set of operating signals, and to provide a triggering signal subsequent to a generation of said first data in response to said trigger instruction signal; and providing a debugging unit operable to transition from said first operating state to said second operating state in response to said triggering signal (column 5, line 54 – column 6, line 20).

Allowable Subject Matter

6. Claims 40, and 43 are allowed.

7. Claims 5, 6, 9, 10, 15-16, 19-20, 23, 25, 30, 34-35, 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed 5/10/2004 have been fully considered but they are not persuasive.

Applicants argue that Miyamori fails to teach any other operating state of the debug module than a transition between a normal state and a debug state. The examiner does not argue this point; however, all rejected claims cite only the transition from a first operating state to a second operating state. Examiner cites the argument of the applicant wherein it is stated "Miyamori teaches a processor core 20 having only one operating state when triggered by an interrupt or exception request from the debug module 30 to <u>transition from the normal mode to the debugging mode</u> ... [emphasis added] (page 29, paragraph 2). The examiner contends that the normal operating state in transition to the debug operating state fulfills the argued limitation of the present application of a transition from one operating state to a second operating state. If the applicant wishes to include the argued limitations of additional operating states, those states must be in the claim language. Therefore, all applicable rejected claims stand.

Applicant also argues that Miyamori fails to teach a processor core distinct from the debugging unit. The examiner fails to find that distinction in the claim language of the argued claims.

Applicant further argues that Miyamori does not teach wherein the trigger instruction is embedded in the instruction stream. The examiner respectfully disagrees. Miyamori teaches that the transition to happen from normal mode to the debugging mode through a hardware break, software break, or debug interrupt (column 6,lines 8-12). Miyamori further teaches "The software break function produces a software break instruction to generate a debug exception... (column 6, lines49-51). The break is internal to the software instruction stream. Therefore, all applicable rejected claims stand.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (703)305-7599. The examiner can normally be reached on M-F, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703)305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm
June 24, 2004

SCOTT BADERMAN
PRIMARY EXAMINER